Bonding, Packaging, and Integration

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Bonding

● Why?
  – Create channels or cavities
  – Create isolation layers (SOI wafers)
  – Reduce complexity on each chip
  – Packaging

● Methods
  – Anodic bonding
  – Silicon fusion bonding
  – Photopolymers
  – Eutectic bonding
  – Others
    ● Press
    ● Thermocompression metallic
    ● Ultrasonic welding
    ● Seam welding
    ● Laser welding
    ● Low-temp glass bonding
Anodic Bonding

- Also called electrostatic bonding
- Bonds glass to silicon
- Used to reduce temp to reasonable levels
- Performed at about 400 C with about 1.2 kV
- Positive ions in glass drift far away from silicon causing high field at interface
- Pull silicon and glass close together
- Silicon positive, glass negative
- Use glass with similar thermal expansion coefficient
- Cleanliness critical to prevent voids
- Thin metal lines can pass through bond
- Using deposited glass (thin layers) reduce voltage significantly
- Works with e-beamed, sputtered, and spin-on glass
Anodic Bonding

Illustration of a typical anodic bonding apparatus.
Silicon Fusion Bonding

- Silicon to silicon bond, oxides also work
- High physical strength
- Require hydroxyl groups on surface
- 300 to 800 C required for bond with higher anneals temps sometimes required
- Use of low-melting glass allows lower temp bond

Silanol bond  Dehydration  Siloxane network
Epoxy or Polyimide Bonding

- Both conductive and non-conductive types
- Inexpensive and simple
- Lower bond strength
- Can form insulating layer
- Potential decomposition
Eutectic Bonding

- Uses silicon metal alloy (other alloys also) such as Si-Ag, Si-Au, Si-Al
- Silicon dissolves in gold at about 370°C and up
- Relatively low temperature
- Microstructure change allows high reliability, strong bond, good heat dissipation, and thermal stability
- Problems with bonding large areas
Eutectic Point for Si - Au

![Graph showing the eutectic point for Si-Au](image-url)
Other Bonding Methods

- Hardware store methods
- Glues, silicones, etc.
- UV Curable materials
- Photoresists
- Waxes
- Chemical bonding
- Hydrophilic bonding
- The simpler the better!!!
Material Costs

- Cost $/kg
- Materials:
  - Plastics
  - Glass & Ceramics
  - Composites
  - Silicon
  - Metals
  - Cu
  - Au
What Does “Packaging” Mean

- Connections from chip to outside world
- Levels of packaging
  - L0: Features on chip
  - L1: Chip
  - L2: Chip carrier
  - L3: Card
  - L4: Board
  - L5: Cables
General Packaging

- Packaging serves two main functions:
  - Protection of device from working environment
  - Protection of environment from device material and operation

- Protection from environment
  - Electrical isolation or passivation from electrolytes and moisture
  - Mechanical protection to ensure structural integrity
  - Optical and thermal protection to prevent undesired effects on performance
  - Chemical isolation from harsh chemical environment

- Protection from device
  - Material selection to eliminate or reduce host response
  - Device operation to avoid toxic products
  - Device insulation
Basic Package
Packaging

- One of least explored MEMS components
- No unique and generally applicable packaging method for MEMS
- Each device works in a special environment
- Each device has unique operational specs
- **Electrical protection**
  - Electrostatic shielding
  - Moisture penetration (major failure mechanism for biosensors)
  - Interface adhesion
  - Interface stress
  - Corrosion of substrate materials

- **Mechanical protection**
  - Rigidity; must be mechanically stable throughout device life
  - Weight, size, and shape for convenience in handling and operation
Major Issues in MEMS Packaging

- Literature is scarce
  - Proprietary processes
- Up to and exceeding 75% of total cost
- MEMS must often be in direct contact with environment
- Often package must be designed specifically for device
- Reliability
- Media compatibility
- Modularity
- Small quantities
- Release and stiction
- Die handling and dicing
- Stress
- Outgassing
- Testing
- Encapsulation/hermetic seals
- Integration
Basic Packaging Operations

- Backside preparation
- Die separation
- Die pick
- Die attach (a)
- Inspection
- Wire Bonding (b)
- Pre-seal inspection

- Packaging and Sealing (c)
- Plating
- Lead trim
- Marking
- Final Tests
Basic Package Types

- Metal can
- Flat pack
- Dual inline package (DIP)
- Chip Carrier
- Pin Array
Die Separation

- Dies
  - Batch fabrication and parallel processing
  - Chop up device

Die separation results.
Basic Packaging Methods

- Wire bonding used to connect microstructures to macro world
  - Uses variety of metals, Au/Al combination popular

- Flip chips
  - Solder bumps used to attach flipped chip
  - Quick universal connection
  - Allows individual chip optimization
  - Connect dissimilar materials
Package Sealing Methods

- **Hermetic**
  - Welding
  - Soldered lid
  - Glass-sealed lid or top

- **Non-hermetic**
  - Epoxy molding
  - Blob top
MEMS Packaging Introduction

- While MEMS devices are becoming a mainstream technology, packaging them for manufacture and ease of use is not matching development of MEMS proper.
- If MEMS are to become available as COTS (commercial off-the-shelf) components, many steps must be taken by industry to bring the many varied kinds of MEMS devices to a ‘Packaged’ state of commercial viability.
MEMS Packaging

- Black hole for cost models
- Modular packaging needed to span large application areas
- Incorporate methods for testing and design
- No standards exist.
- Just as in the IC and Discrete Electronics world, packaging for MEMS should be standardized for the sake of price and availability wherever possible.
MEMS Packaging

- MEMS will likely follow IC and discrete electronic package forms and types.
- As MEMS become more and more mainstream, semiconductor manufacturers will likely use existing packages and adapt MEMS manufacturing to these well-established commercial form factors wherever the application of MEMS may be accommodated by IC packages which may open an ‘Undiscovered Country’ of applications.
- Not all MEMS devices are electronic in nature and may present challenges in packaging that are not solvable with PWB (printed wiring board) form factors.
MEMS Packaging

- MEMS will likely be electronically coupled with other devices in MCMs (Multi-Chip Module). COTS Semiconductor manufacturers are involved.
- For MEMS to provide optimal functional sensitivity and bandwidth, they may be mounted in MCM–D-C-Ls (Multi-Chip Module, Discrete, Capsule, Local).
- This matching of multiple technologies in a single package is paramount to MEMS technology applications.
- This brings about the need for advanced packaging schemes.
- If a single package houses multiple MEMS, Discretes, and ICs, there stems the dilemma of interfacing the MEMS with the environment (gas, fluids, light, RF, inertia, sound, vibration, biomass, etc.) and still protect the Electronics from the environment.
- The common notion is that most MEMS will be PWB or MCM mounted but this will not always be the case.
MEMS Packaging

- MEMS packaging may vary widely by special function as opposed to electronic packaging for board mounting.
- As MEMS packaging evolves, packaging may specialize to accommodate the special function of the MEMS proper
  - Creates new form factors
- This evolution happens rapidly.
- E-COTS has a rollover of 12 to 18 months often with different packaging.
- As MEMS become more widely available, the need for special packaging will settle down to an accepted array of ‘Package Form Factors.’
- All MEMS are not electronics-based, but are indeed small mechanical devices
MEMS Packaging

- Recent data gathering indicates a burgeoning effort to package MEMS for E-COTS.
- MEMS technology promises to integrate many electronic circuits ‘On Board’ and use popular E-COTS packaging technologies.
- Even though MEMS have been a laboratory curiosity for years, they are only now becoming mainstream discrete-packaged products.
MEMS Packaging

- MEMS technology lends itself to Flip-Chip & Un-Flip-Chip, back-etched thinned silicon with through-hole vias, and Direct-Chip-Attach application.
- Whether attaching ICs to a MEMS substrate, attaching MEMS to an IC, or mounting MEMS, ICs and Discretes in an MCM, the possibilities of converging technologies for integrating MEMS and Electronics deserves great attention.
MEMS Packaging Lead Frame

Cross-Section of MEMS Acoustic Sensor packaged with a preamp die.
MEMS Packaging Surface Mount

Cross-Section of MEMS Pressure Sensor packaged with a signal conditioning die.
MEMS Packaging Ceramic

Fine Pointing Mirror for Space-born Applications

[Diagram showing MEMS packaging with labels for Silicon chip, Coated mirror surface, Metal shield, Glass base, Contacts, Support plate, Reflecting Surface of Micro Moving Mirror MEMS, Window, Light, Moving Mirror MEMS, Glass Base, Ceramic Support Plate]
MEMS Packaging Roadmap

1. Product Specific Unique Package
2. 28 Pin CERDIP
3. Hermetic Firewall
4. Flip Chip
5. BGA
6. Air Bag Sensor
7. InkJet Print Cartridge
8. Photo and Voltaic
9. Pressure Sensor
10. Oxygen Sensor
11. Ultra-Thin Chip Stack
12. Microphone w Hybrid Amp
13. Plastic Cap
14. Metal Cap
15. Cavity
16. Chip on Chip
17. Chip in Cavity
18. MEMS on Chip
19. Chip on (in) MEMS
MEMS Application Domain Map

Chart of Number of Transistors Versus Number of Mechanical Components
MEMS Packaging – MEMS Software Design

RF & Microwave Board Design Software

http://www.mwoffice.com
MEMS Packaging – MEMS Design Software

Gas, Fluid, Mechanical, 3D Geometry, & Package Modeling

Observe complete solution from Left to Right, Valve - Pump - Router – Dual In-line Package

Note - Can be made available in other package forms such as BGA (Ball Grid Arrays).

http://www.cfdrc.com/
MEMS Packaging – Thermal Modeling

**THERMO MODEL**

Fast and accurate model generation, based on dynamic thermal responses either measured or simulated.

**FEM results**

**THERMO MODEL results**

[MicReD](http://www.micred.com/)
MEMS Packaging – Embedded Interconnection

3D integration of embedded back-side-thinned IC into multi-layer interconnection substrate structure onto which may be mounted a MEMS for interconnect.

Re-metalized and Planarized back-side-thinned IC

Pocket Edge

Multi-layer interconnect substrate with cavity housing thinned IC

Multi-layer interconnect metalization

Chip-Substrate interface
MEMS Packaging Issues

- Primary packaging types – Caps & Cavities
- Secondary packaging types – IC type packages & Custom
- **Barrier to Commercialization is Packaging**
- Barriers are falling
- Package must be inexpensive, capable of being handled by existing automated board assembly machinery, and capable of protecting the MEMS against contamination
- Each of the many package technologies has its own performance characteristics and associated price
- Defining package performance requirements is the key to selecting the correct package for a given application
- The package design must protect the MEMS at the wafer level and may involve an extra step or more in the fabrication process
MEMS Packaging Issues - Cap Wafers

Steps of Packaging Cap Wafers


2. Silicon Capped Micro-Machine die with gel-coat protection.

3. In a MEMS SOIC (Small Outline IC Plastic Package) package the thickness is non-standard.
MEMS Packaging Issues – Cavity Packs

Varieties of Cavity-Molded Packages

1. Standard CERDIP, cavity leaded package Solder-seal DIL package
   - Frit Glass Seal
   - Solder Seal or Ceramic Frit Seal Lid

2. SO Pre-molded Cavity Package Array-assembled epoxy-dam cavity package
   - Ceramic, Metal or Organic Lid
   - Epoxy Seal
   - Pre-molded Plastic Body (Transfer Injection)
   - Liquid Encapsulant
   - Ceramic or Laminate

3. LCC snap-array cavity package
   - Solder Seal, Frit or Epoxy
   - Ceramic Snap Element

Not to Scale
MEMS Packaging Issues – PWB and MCM

High Performance Module
Intermediate Packaged Device

Cu/Ag Ball or Flat Grid Array

Epoxy-filled Cavity

Encapsulation (Optional)

Underfill not shown

Cut-Away Side View

Si Substrate

Known Good Die

Embedded Discretes
(MEMS future)

A few larger discretes could also be mounted on the Si Substrate

Legend:  
Cu - Copper
Ag - Silver
Si - Silicon

Mixed Technology PWB

CSM/MCM
Intermediate Packaged Device
(DCA Flip-Chip with ASICs)

Larger Discretes, connectors and add-on MEMS or MIC

DCA - CSM/MCM
(Super Flip-Chip On PWB)

Large ASIC - DCA
MEMS Packaging Issues – Summary

- If the MEMS devices is truly robust, the lowest-cost package may be from standard IC package types.
- The MEMS is not quite robust enough to withstand injection molding, the gel coat method or some lower stress method may be employed.
- To Package MEMS, there will be tradeoffs in terms of cost versus environmental resistance.
- There will still be a requirement for custom form factors such as may be used to package non-electronic MEMS.
Packaging Materials

- **Silicone**
  - Excellent for short-term encapsulation
  - Medical-grade silicone is biocompatible
  - Easy to apply and sterilize
  - Excellent adhesion characteristics; flexible
  - Swells in most aqueous solutions
  - Air bubble entrapment is a problem

- **Polyurethane**
  - Good humidity and chemical resistance
  - High dielectric strength
  - Good mechanical properties, flexible
  - Attacked, swollen, or dissolved by many solvents
Packaging Materials

- **Epoxy**
  - Good mechanical properties
  - Poor ion and moisture barriers
  - Shrink when cured, changing mechanical, electrical, thermal properties

- **Fluorocarbon**
  - Most well known (polytetrafluoroethylene)
  - Desirable electrical characteristics
  - Poor adhesion and mechanical characteristics

- **Acrylic**
  - Good electrical properties
  - Hard, rigid, and tough
  - Little shrinkage during cure
  - Poor solvent resistance
Packaging Materials

- **Parylene**
  - Can use CVD to deposit thin, uniform pinhole-free films
  - Good electrical properties
  - Low permeability to moisture and gases
  - Poor adhesion

- **Polyimide**
  - Good mechanical and electrical properties
  - Stable over wide range of temperatures
  - Commonly used in microelectronics

- **Glass**
  - Thermal expansion coefficients must be matched
  - High strength, especially in compression
  - Good electrical properties
  - Localized stress concentrations due to surface imperfections
Packaging Materials

- Ceramic
  - Chemically inert
  - Brittle, low fracture toughness
  - Good electrical properties
  - Excellent moisture barrier
  - Require high temperature for sealing
  - Typically biocompatible

- Metal
  - Light weight
  - Some metals (e.g., titanium) have excellent corrosion resistance
  - Good mechanical properties
Die Attach Materials

- Conducting
  - Gold / silicon eutectic
  - Metal filled epoxy
  - Conducting polyimide

- Non-conducting
  - Epoxy adhesive
  - Insulating polyimide
Designs that Consider Manufacturing, Packaging and Testing will get to Market Quicker

Traditional process:
- Concept: 5%
- Detail: 25%
- Changes: 55%
- Data: 15%

DµMPT process:
- Concept: 20%
- Detail: 15%
- Changes: 15%
- Data: 5%

45% Savings
MEMS Packaging - Bibliography

- Home of the IEEE Computer Society http://www.computer.org/
- CFD Research Corp. Home Page http://www.cfdrc.com
- Applied Wave Research http://www.mwoffice.com
- Design, Test, Integration, and Packaging of MEMS/MOEMS
  - Volume 4019
- SPIE-The International Society of Optical Engineering
- ISBN 0-8194-3645-3
- ECN, Vol. 44, No. 6 http://www.ecnmag.com
System Integration

- Interfacing of electronics with sensors/actuators
  - (decision making capability or intelligence)
Monolithic Integration

Integration of chemical, mechanical, biochemical or optical microsystems with electronics

circuit design and simulation
circuit fabrication at a foundry

fabricated microsystem on a chip with circuits

Gas sensor

Accelerometer
System Integration

- Pre-IC fabrication
- Co-IC fabrication
- Post-IC fabrication

Post-IC fabrication requires:
- Low temperature < 450°C
- Benign chemical environment
Summary of steps

• Circuit design and simulation
• CMOS circuit fabrication at foundry
• Co- and Post-IC MEMS fabrication
• System packaging
Hybrid or Modular Integration

MEMS pressure sensor array

Micrograph of pressure sensor array